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10/716,913	11/18/2003	Mitchell S. Fletcher	H0004377--1622	6411

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HONEYWELL INTERNATIONAL INC.
101 COLUMBIA ROAD
P O BOX 2245
MORRISTOWN, NJ 07962-2245

EXAMINER	
SZETO, JACK W	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,913	FLETCHER ET AL.	
	Examiner	Art Unit	
	Jack W. Szeto	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/18/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Official Action

Status of the Specification and Claims

Claims 1-5, 7-9 and 12 are rejected under 102(b).

Claims 6, 10-11, and 13-18 are rejected under 103(a).

Claims 1-7 are objected to based on minor informalities.

Claim Objections, Minor Informalities

Claims 1-7 are objected to because of the following informalities:

As per claim 1, interface is repeated. Appropriate corrections are recommended. Claims 2-7 inherit this objection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Garnett (United States Patent No. 5,991,900).

As per claim 1, Garnett discloses:

A bus isolator for coupling a bus of a first predetermined configuration and signaling protocol to a peripheral via an input/output (I/O) circuit of a second predetermined configuration and signaling protocol [column 4, lines 1-15: bridge couples P buses to D bus. These buses can be any configuration. The bridge is functionally equivalent to the isolator.], comprising:

a first interface adapted to couple to the bus [Figure 6, reference 24 or 26];

a second interface interface adapted to coupled to the I/O circuit [Figure 6, reference 82 and column 4, lines 16-20: SCSI or E-NET interfaces (I/O circuit)];

a controller coupled to, and receiving signals from, the first and second interfaces [Figure 6, reference 90];

a memory coupled to the controller for storing the signals received from the first and second interfaces [Figure 6, reference 126] and

a processing element coupled to the controller and the memory for managing the activity of the isolator [Figure 6, reference 88],

wherein data is transmitted from the I/O circuit to the bus only in response to a data request from the bus [column 19, table 2: in one configuration, data from D interface is only transmitted the bus (PA or PB) makes a request (read)].

As per claim 2, Garnett discloses:

The isolator of claim 1 wherein data requested by the bus from the I/O circuit is sent via the second interface to the memory and the processor, where the integrity of the requested data is verified and only sent to the bus if it is appropriately formatted, whereby a defective I/O circuit or a defective peripheral coupled to the I/O circuit cannot capture the bus [column 12, lines 24-

33 and column 7, lines 48-55: data verified for read request from processing set (bus) and data is caught in the bridge].

As per claim 3, Garnett discloses:

The isolator of claim 1 wherein the I/O circuit is a commercially available I/O circuit [column 4, lines 15-20: ENET and SCSI interfaces are commercially available].

As per claim 4, Garnett discloses:

The isolator of claim 1 wherein the bus is a commercially available bus [column 3, line 66 to column 4, line 5: PCI buses are commercially available].

As per claim 5, Garnett discloses:

The isolator of claim 1 wherein the memory comprises an isolation memory, having a first portion wherein data is received from the first interface and a second portion where data is received from the second interface [column 10, lines 47-55: all writes (from both interfaces) are written to the posted write buffers].

As per claim 7, Garnett discloses:

The isolator of claim 1 wherein the processing element comprises a state machine, a simple controller, a microprocessor, a digital signal processor or a combination of first and second lock-step processors [Figure 6, reference 88 and Figure 8, reference 132: a controller].

As per claim 8, Garnett discloses:

An electronic system, comprising:

a plurality of peripherals [Figure 1, references 28, 29 and column 4, lines 16-19: devices (peripherals) are attached to SCSI or E-NET interfaces];

a plurality of I/O elements, each coupled to one of the peripherals for passing signals to and from the one of the peripherals [Figure 1, references 28, 29 and column 4, lines 16-19: devices (peripherals) are attached to SCSI or E-NET interfaces (I/O elements)];

a plurality of isolation elements, each coupled to at least one of the I/O elements for passing signals to and from the at least one I/O element [Figure 2 and column 4, lines 32-34: plurality of bridges coupled to at least one I/O element]; and

a bus coupled to each isolation element for sending commands and output data to, and receiving requested input data from, the peripherals via the isolation elements and the I/O elements [Figure 1 and 2];

wherein each isolation element comprises:

a target interface coupled to the bus for receiving the commands and output data from, and transmitting the requested input data to, the bus [Figure 6, reference 24 or 26];

a master interface coupled to the at least one of the I/O elements for transmitting the commands and output data to, and receiving the requested input data from, the peripheral [Figure 6, reference 82 and column 4, lines 16-20: SCSI or E-NET interfaces (I/O circuit)];

a controller coupled to the target interface and the master interface for controlling transmission of the commands, the input data, and the output data there between interfaces [Figure 6, reference 90];

a memory coupled to the controller for receiving the commands, the output data, and the requested input data [Figure 6, reference 126]; and

a processor coupled to the memory and the controller for managing command and input and output data flow between the bus and the at least one I/O element [Figure 6, reference 88].

As per claim 9, Garnett discloses:

The system of claim 8 wherein the memory comprises an isolation memory having one part coupled to the at least one I/O element for receiving data transfer therefrom and another part coupled to the bus for receiving command and data transfer therefrom [column 10, lines 47-55: all writes (from both interfaces) are written to the posted write buffers].

Claims 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogura (United States Patent No. 6,145,044).

As per claim 12, Garnett discloses:

A method for coupling a bus and a peripheral via an isolator [Figure 1: bridge equivalent to isolator], comprising:

determining whether there is a message on the bus for the peripheral [column 11, line 58 to column 12, line 33: determining whether signal is read or write I/O];

temporarily storing the message in the isolator [column 11, line 58 to column 12, line 33: comparator (on bridge) compares signal, thus the signal (message) must be stored];

determining whether the message is for output to the peripheral or input from the peripheral [column 11, line 58 to column 12, line 33: determining whether signal is read (input) or write (output) I/O]; and

if for output to the peripheral, sending the output to the peripheral [column 11, line 58 to column 12, line 33: data written to D bus for device]; and

if for input from the peripheral;

requesting the input from the peripheral [column 11, line 58 to column 12, line 33: receiving read data from device];

receiving the input from the peripheral and temporarily storing it in the isolator [column 11, line 58 to column 12, line 33: receiving read data from device];

checking the input from the peripheral [column 12, lines 24- 33 and column 7, lines 48-55: data verified for read request from processing set (bus) and data is caught in the bridge]; and

if valid, transferring the input from the peripheral to the bus [column 12, lines 24- 33 and column 7, lines 48-55: data verified for read request from processing set (bus) and data is caught in the bridge]; and

if not valid, not transferring the input from the peripheral to the bus [column 12, lines 24- 33 and column 7, lines 48-55: data verified for read request from processing set (bus) and data is caught in the bridge].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett (United States Patent No. 5,991, 900), and further in view of Jones (United States Patent No. 5,729,767).

As per claim 6, Garnett does not discloses:

The isolator of claim 5 wherein the memory further comprises *a program memory and a flash memory.*

Jones discloses:

The isolator of claim 5 wherein the memory further comprises a program memory and a flash memory [column 1, lines 39-43: flash memory coupled to processor to include firmware (program and configuration)].

Both Garnett and Jones disclose controllers (bridges) in data transfer systems. Garnett does not explicitly disclose having the memory in his bridge (controller) comprising of program and flash memory. However, Garnett's bridge control logic [Garnett, Figure 8 and from column 8, line 13] must contain programming which is executed to perform its task. Having the memory comprising of program and flash memory makes upgrading easier and more cost effective [Jones, column 1, lines 40-44]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a program and flash memory as taught in Jones into memory of the system of Garnett to make upgrading easier and more cost effective.

As per claim 10, Garnett does not discloses:

The system of claim 9 wherein the memory further comprises program memory containing programs for execution by the processor and flash memory for containing configuration data for the isolation element [column 1, lines 39-43: flash memory coupled to processor to include firmware (program and configuration)].

Both Garnett and Jones disclose controllers (bridges) in data transfer systems. Garnett does not explicitly disclose having the memory in his bridge (controller) comprising of program and flash memory. However, Garnett's bridge control logic [Garnett, Figure 8 and from column 8, line 13] must contain programming which is executed to perform its task. Having the memory comprising of program and flash memory makes upgrading easier and more cost effective [Jones, column 1, lines 40-44]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate a program and flash memory as taught in Jones into memory of the system of Garnett to make upgrading easier and more cost effective.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett (United States Patent No. 5,991,900), and further in view of Miyamori (United States Patent No. 5,978,937).

As per claim 11, Miyamori discloses:

The system of claim 8 further comprising a debug port coupled to the processor [Figure 4 and 5: debug module coupled to the processor includes ports].

Garnett discloses a system with a bridge that includes a controller (processor). However, Garnett does not disclose having a debug port coupled to the processor. Miyamori discloses a debug port coupled to a processor for better maintenance and monitoring [column 2, line 53 to column 3, line 7: less complex method of monitoring]. Having a debug port coupled to the processor is well known in the art and allows for maintaining and monitoring of the bridge. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to couple a debug port to the processor as taught in Miyamori into the system of Garnett to create a more maintainable system.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett (United States Patent No. 5,991,900), and further in view of Kanemaru (United States Patent No. 6,341,334).

As per claim 13, Kanemaru discloses:

The method of claim 12 further comprising before the first sending step, *determining whether the output for the peripheral is in the message or already stored in the isolator.*

Kanemaru discloses:

determining whether the output for the peripheral is in the message or already stored in the isolator [column 9, lines 8-35: determines whether data needed to be transferred is store in cache locally]

Both Garnett and Kanemaru disclose using bus bridges for handling I/O request to/from peripherals. Garnett does not disclose caching data and checking a local memory (on the bridge) for the data before sending it to/from the bridge. Garnett does disclose temporarily storing data in write posted buffers, however, Garnett does not explicitly disclose checking these write posted buffers and transferring the contents when there is a data request. Kanemaru, on the other hand, explicitly discloses storing data locally in the bridge and checking to see if the data exist on the bridge first. Caching data and determining if the data is stored locally increases efficiency [column 1, lines 60-64]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the enhanced features of caching and checking local storage for a copy of the data before sending it out as taught in Kanemaru into the bus bridge of Garnett to create a more efficient data transfer system.

Claims 14-15 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett (United States Patent No. 5,991,900) and Kanemaru (United States Patent No. 6,341,334), and further in view of Datwyler (United States Patent No. 5,509,127).

As per claim 14, neither Ogura nor Kanemaru discloses.

The method of claim 13 wherein if the output for the peripheral is already in the message, further comprising *determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not free setting an error indicator.*

Datwyler discloses:

determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not free setting an error indicator [column 2, lines 44-60: determining if bus is busy, if it is error is generated].

The systems disclosed by Datwyler, Garnett, and Kanemaru teaches handling of data transfer. Neither Garnett nor Kanemaru explicitly teach determining whether a bus is free or not. Determining whether a bus is free and indicating an error if it is not, is well known in the art and increases the reliability of the transmission of data [Datwyler, column 2, lines 22-50: insure data integrity]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the method of determining whether a bus is free as taught in Datwyler into the system of Garnett and Kanemaru to create a more reliable data transfer system.

As per claim 15, Garnett does not disclose:

The method of claim 13 wherein *if the output for the peripheral is already stored in the isolator, further comprising retrieving the stored output* and *determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not*

free setting an error indicator.

Kanemaru discloses:

if the output for the peripheral is already stored in the isolator, further comprising retrieving the stored output [column 9, lines 8-35: determines whether data needed to be transferred is store in cache locally].

Both Garnett and Kanemaru disclose using bus bridges for handling I/O request to/from peripherals. Garnett does not disclose caching data and checking a local memory (on the bridge) for the data before sending it to/from the bridge. Garnett does disclose temporarily storing data in write posted buffers, however, Garnett does not explicitly disclose checking these write posted buffers and transferring the contents when there is a data request. Kanemaru, on the other hand, explicitly discloses storing data locally in the bridge and checking to see if the data exist on the bridge first. Caching data and determining if the data is stored locally increases efficiency [column 1, lines 60-64]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the enhanced features of caching and checking local storage for a copy of the data before sending it out as taught in Kanemaru into the bus bridge of Garnett to create a more efficient data transfer system.

As per claim 15, neither Ogura nor Kanemaru discloses.

determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not free setting an error indicator.

Datwyler discloses:

determining whether a bus coupling the peripheral to the isolator is free and if free sending the output to the peripheral and if not free setting an error indicator [column 2, lines 44-60: determining if bus is busy, if it is error is generated].

The systems disclosed by Datwyler, Garnett, and Kanemaru teaches handling of data transfer. Neither Garnett nor Kanemaru explicitly teach determining whether a bus is free or not. Determining whether a bus is free and indicating an error if it is not, is well known in the art and increases the reliability of the transmission of data [Datwyler, column 2, lines 22-50: insure data integrity]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the method of determining whether a bus is free as taught in Datwyler into the system of Garnett and Kanemaru to create a more reliable data transfer system.

As per claim 17, Datwyler discloses:

The method of claim 16 further comprising after the sending step, checking to see whether the sending step was successful [Column 10, lines 42-47: signal to indication bus operations was completed successfully].

As per claim 18, Datwyler discloses

The method of claim 12 further comprising after the transferring step, checking to see whether the transferring step was successful [Column 10, lines 42-47: signal to indication bus operations was completed successfully].

The systems disclosed by Datwyler, Garnett, and Kanemaru teaches handling of data transfer. Neither Garnett nor Kanemaru explicitly teach determining if the transaction has completed successfully, while Datwyler does. Determining if a bus transaction has completed successfully allows for better error handling. If a transaction was not successfully, the system can implement a corrective action. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the method of determining whether a transaction was completed successfully as taught in Datwyler into the system of Garnett and Kanemaru to handle errors better.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garnett (United States Patent No. 5,991,900), and further in view of Kang (United States Patent Publication No. 2003/0093746).

As per claim 16, Garnett discloses:

The method of claim 12 wherein the checking step comprises determining whether the input from the peripheral *is timely* and valid and *if timely* and valid sending the input from the peripheral to the bus and *if not timely* and valid setting an error indicator [column 12, lines 24-33 and column 7, lines 48-55: data verified for read request from processing set (bus) and data is caught in the bridge].

Garnett does not discloses:

The method of claim 12 wherein the checking step comprises determining whether the input from the peripheral *is timely* and valid and *if timely* and valid sending the input from the peripheral to the bus and *if not timely* and valid setting an error indicator.

Kang discloses:

determining whether the input from the peripheral *is timely* and valid and *if timely* and valid sending the input from the peripheral to the bus and *if not timely* and valid setting an error indicator [para 0020: transmission error when data is not received in time].

Both Kang and Garnett teach data transfer system. While Garnett teaches determining whether the data received is valid, Garnett fails to teach whether if the data is transmitted in a timely manner. Kang discloses a system where if data is not received in time, it is considered an error. Determining if data is received in a timely manner increases the chance of catching transmission errors. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the method of determining if data was transmitted in a timely manner as taught in Kang into the system of Garnett for better error handling.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack W. Szeto whose telephone number is (571) 272-1537. The examiner can normally be reached on M-F 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jws

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER